4-bit BCD Counter with 7-Segment LED Display

Lab 3 ENEE 245

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**Objective**:

4-bit BCD counter will be developed to simulate counting on a 7-segment Common Anode LED Pin Layout. The counter needs testing after building the circuit online as well as physically. Combining other gates for a functional counter is required with diagrams.

**Design**:

Use JK flipflop (7476) or D flipflop (7474) to develop a 4-bit Binary Coded Decimal counter. The counter starts at 0 (0000) and must return to 0 after reaching 9 (1001). Present state and next state binary numbers are listed:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Present State | Next State | JK A | JK B | JK C | JK D |
| 0 | 0000 | 0001 | 0X | 0X | 0X | 1X |
| 1 | 0001 | 0010 | 0X | 0X | 1X | X1 |
| 2 | 0010 | 0011 | 0X | 0X | X0 | 1X |
| 3 | 0011 | 0100 | 0X | 1X | X1 | X1 |
| 4 | 0100 | 0101 | 0X | X0 | 0X | 1X |
| 5 | 0101 | 0110 | 0X | X0 | 1X | X1 |
| 6 | 0110 | 0111 | 0X | X0 | X0 | 1X |
| 7 | 0111 | 1000 | 1X | X1 | X1 | X1 |
| 8 | 1000 | 1001 | 0X | 0X | 0X | 1X |
| 9 | 1001 | 0000 | X1 | 0X | 0X | X1 |

K-maps were calculated by hand and are follows:

* JA = BCD
* KA = D
* JB = CD
* KB = CD
* JC = A’D
* KC = D
* JD = 1
* KD = 1

These equations stem from the eight columns of JK flipflops. Each column was placed into a K-map and simplified to get the equations above.

Diagram, schematic

Description automatically generated

Figure 1: Circuit Implementation with Quartus II software

**Hardware**:

* Oscilloscope
* 8 resistors
* 2 JK flipflop 7476
* NAND Chip 7400
* Transistor 7404
* Binary Coded Decimal (BCD) 7447
* 7-segment Decoder
* Function Generator
* Power Supply

**Experiment**:

JK flipflops (7476) were chosen as the gate way to complete the circuit. The inputs needed varies combinations such as JC equaling A’D and JA requiring BCD. Chips NAND (7400) and Transistor (7404), both require one unit for achieving K-map logic. Once all the chips are grounded and positioned positively figurative and literally QA, QB, QC, and QD needed to produce correct outcomes. Clock pins for each chip were manipulated, all connecting to the function generator. On to the inputs, JD and KD are connected to positive notches on the breadboard. Now QD’s is connected to KA and KC with two separate wires. QD is also combine with QA (via 4700) which has gone through a transistor and travel through a transistor one final time returning A’D. QC and QD go into NAND then a transistor producing CD, CD is plugged into JC and KC. Finally, CD is combined with QB via NAND chip and transistor for pin JA.

Chart, box and whisker chart

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Figure 2: Oscilloscope displays QA/D0, QB/D1, QC/D2, and QD/D3.

In figure 2, logically construction may be verified by counting each section of the timer. The count begins at 8, continues to 9, and returns to 0. The counted maintains counting until 9 and repeats the cycle again.

Diagram

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Figure 3: The breadboard is fully powered on displays current count of 9 on the 7-segment LED visual

Once outputs from the clock are verified on the oscilloscope via figure 2 QA, QB, QC, and QD are connected to the Binary Coded Decimal decoder as inputs. Also, ground and connect to corresponding positive ends. Output from the decoder can be attached to the 7-segment display, each output is required for a specific pin. Below, figure 4 entails the procedure to connect the decoder to the display. I used this image to join the proper pins correctly. The connection are as follows (decoder to display):

* Pin 9 to 5
* Pin 10 to 6
* Pin 11 to 8
* Pin 12 to 10
* Pin 13 to 1
* Pin 14 to 9
* Diagram, schematic

  Description automatically generatedPin 15 to 2

A picture containing text, clock

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Figure 4: From the Experiment section on Lab 3, BCD to 7-segment Decoder.

Diagram

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Figure 5: The breadboard is fully powered on displays current count of 3 on the 7-segment LED visual

Diagram

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Figure 6: The breadboard is fully powered on displays current count of 6 on the 7-segment LED visual

**Analysis**:

There is no count error on the oscilloscope as well as the 7-segment display. I developed a synchronous counter using the two JK flipflops, a NAND chip, and a transistor. The ripple/asynchronous counter is more prone to error because each flipflop is not individually clocked together. I encountered troubles starting out the circuitry, unsure what exactly is used for the input and output. Subsequently, Professor Xiang help initiate the process and made the procedure clearer. I had a refresher in JK flipflops and able to build a repetitive counting system.

**Conclusion**:

Constructing a display counter is much simpler than it seems. JK flipflops allows data to pass through as an output with requirements. Criteria creates a path for any data to display and can develop a counting system. 4-bit binary numbers can be manipulated to repeat or change. Overall, I created a counter system with JK flipflops, NAND gate, transistor, binary decoder, and an arrangement. Final product counted continuously from 0 to 9. I learned wiring criteria for JK flipflops and installing decoder with a 7-segment display.